

### Course Abstract

The USB System Architecture class is an in-depth discussion of USB and is based on the 2.0 version of the Universal Serial Bus specification. This course covers the operation of low-, full-, and high-speed USB devices as well as host system requirements (including UHCI, OHCI, and EHCI implementations). It includes a discussion of the Universal Transceiver Macrocell Interface for high-speed designs, and covers the On-the-Go implementations, but focuses on the protocol, signaling environment, and electrical specifications, along with the hardware/software interaction required to configure and access USB devices. The course also includes protocol analyzer demonstrations and debugging techniques. MindShare's established background in PC Architecture and comprehensive understanding of IEEE 1394 and other technologies (including PCI-X 2.0, InfiniBand, and HyperTransport) provides rich insight into USB and results in a superior training experience for our customers. This course provides in-depth information, example implementations, and practical guidance that will give you a running start on your design.

### Course Content

- USB Design Goals
- Introduction to USB Concepts
- USB Hardware/Software Model
- Transfer Types & Scheduling
- Packets & Transactions
- Error Recovery
- Physical Layer
  - o Full Speed/Low Speed
  - o High Speed
- Hub Overview
  - o Full-Speed/Low-Speed Hubs
  - o High-Speed Hubs & Split Transactions
- USB System Architecture
  - o Configuration Process
    - o Descriptors, Enumeration, High-Speed Detection
    - o Compound and Composite Devices
  - o Device Software Overview
  - o USB Host Software Overview
    - o Identifying devices and binding drivers (Windows ".inf").
    - o How the Host manages composite devices.
  - o USB Device Classes
    - o Human Interface (HID)
    - o Mass Storage
    - o CDC (ACM, ECM, OBEX)
    - o PictBridge and MTP (both are based on SICD)

### Course Content ( Continued )

- o Cables and Connectors
- o Power Delivery and Low Power Modes
  - o Includes latest changes for 2.5mA suspend mode current and optional “quick entry” low power state.
- USB Specification Extensions
  - o USB On-The-Go and Embedded Hosts.
  - o Inter-Chip USB (For both Full-Speed and High-Speed).
  - o USB Battery Charging ECN.
- Advanced Topics
  - o Physical Layer Implementation Options
    - o UTMI, UTMI+, ULPI, “classic” 7-pin PHY Interface
  - o USB Host/Device Hardware Architecture
  - o Hub Details
  - o Hub Configuration
  - o Hub Operations
  - o Full-Speed/Low-Speed Hubs
  - o High-Speed Hubs & Transaction Translators
  - o Host Controllers
    - o Universal Host Controller Interface (UHCI)
    - o Open Host Controller Interface (OHCI)
    - o Enhanced Host Controller Interface (EHCI)

### Who Should Attend

This in-depth course is designed with the hardware or software engineer in mind. The course contains practical examples of USB transactions and error conditions. It describes all the rules required for a device to be specification compliant. This makes the course ideal for a system validation engineer who validates RTL-level, chip-level, system-level or system board-level designs.

### Recommended Prerequisites:

A fundamental understanding of PC Architecture is a prerequisite.

### Corresponding Book:

MindShare’s [USB System Architecture Textbook](#) (2nd Edition)

Author: Don Anderson Publisher: Addison Wesley

**Trainer : Mike Kentley**



**Mike Kentley** currently teaches for MindShare, Inc as a consultant from High Desert Design Center (HDDC), a company he founded. An industry veteran, Mike ensures that HDDC clients receive high performance, functionally accurate designs in today's short time to market environment.

Mike Kentley helps companies achieve first pass success with their products. Mike works one-on-one with clients on advanced SoC and FPGA design and verification projects, specializing in Universal Serial Bus (USB) and PCI Express. Over the last ten years, Mike has worked with clients ranging from startups to Fortune 500 companies, delivering a wide range of deliverables such as:

- Hardware architecture specifications.
- USB and PCI Express design and verification implementation.
- Embedded software development.
- New product debug and troubleshooting.
- Custom embedded USB training material.
- Complete verification environments and test suites.
- Training in USB and PCI Express technology

The wide range of clients and projects has allowed Mike to develop his expertise in teaching, hardware architecture definition, design, verification, firmware development, microprocessors, storage products, and a host of other applications. Mike specializes in Universal Serial Bus and PCI Express product development on SoC and FPGA. He is an expert RTL and verification testbench developer, working in Verilog, VHDL, e and SystemVerilog.

<b>Course Date</b>	29 Jul – 1 Aug 2008 ( 4 Days ) 9am to 5pm Lunch Time from 12pm to 1pm
<b>Course Venue</b>	<b>PSB Academy's Delta Campus</b> 355 Jalan Bukit Ho Swee Singapore 169567
<b>Course Fee</b>	S\$3200 per pax Discount of S\$300 for registration before <b>21 Jun 08</b> Discount of S\$200 for group of 3 or more Training note will be provided. Lunch not included.
<b>Payment Term</b>	Payment in advance Mode : Cheque or Bank Transfer or Paypal
<b>Register To</b>	Mr J.K Tan Spyro Technology 14 Holland Avenue #14-55 Singapore 271014
<b>Email To</b>	<a href="mailto:jktan@spyrotechnology.com">jktan@spyrotechnology.com</a>
<b>Contact Us</b>	Tel/Fax : (65)-6778 0948 Mobile : (65)-96688007
<b>Term &amp; Condition</b>	Spyro Technology reserves the right to cancel a course for any reason, including insufficient enrollment. If a course is cancelled, all registration fees will be refunded.